REMARKS

Entry of this amendment prior to examination and in supplement to the Preliminary Amendment filed on July 28, 2003 is respectfully requested.

By the present amendment, claim 13 is also cancelled, in addition to the previously cancelled claims 3-12 and 20-28 so that examination can proceed on claims 1, 2, 14-19 and 29-33. Also minor amendments have been made to the claims for purposes of clarification.

With regard to the pending claims 1, 2, 14-19 and 29-33, it is respectfully submitted that these claims define over the cited references set forth in the August 9, 2002 Office Action in the parent application. In each case, the independent claims 1, 14 and 29 define features neither taught nor suggested in the cited prior art from the August 9, 2002 Office Action.

For example, with regard to the independent claim 14, an arrangement is set forth with first and second bit lines and first and second redundant bit lines operating in conjunction with memory cells and redundant memory cells a first amplifier and a first redundant amplifier:

> "wherein said first bit line is to be replaced with said first redundant bit line but said second bit line is not to be replaced with said second redundant bit line."

As discussed on page 37, lines 9 et seq. of the specification, this feature has the important advantage of enhancing use efficiency of the redundant bit lines in the system. In particular, it permits making it "possible to replace a failed bit line with a redundant bit line and the corresponding redundant sense amplifier on a bit-line basis of the bit-line pair." (see page 37, lines 18 et seq.)

Claim 1 defines this from a different perspective in terms of the latch circuits having input/output nodes "connected to half of the bit line pairs provided to each of said memory mats." In conjunction with this, claim 1 defines:

> "wherein a failed bit line of said bit line pairs can be replaced, on a bit-line basis, with a redundant bit line and a corresponding redundant sense amplifier."

Again, this creates the effect of enhancing the use efficiency of the redundant bit lines, as discussed on page 37, line 9 et seq.

In a similar manner, claim 39 defines the invention in terms of first and second normal bit lines, first and second redundant bit lines, first and second normal memory cells, first and second redundant memory cells, a plurality of first amplifier circuits and a second amplifier circuit, as well as an information hold circuit:

> "said information hold circuit replacing one of said first normal bit lines with said first redundant bit line but not replacing one of said second normal bit lines corresponding to said one of said first normal bit lines with said second redundant bit line."

Again, this permits the same enhancement of use efficiency discussed above with regard to claims 1 and 14.

Although the prior art cited in the August 9, 2002 Office Action in the parent application is of general interest, it is respectfully submitted that none of the cited references teach or suggest the above noted features from the independent claims 1, 14, and 29. Accordingly, it is respectfully submitted that these independent claims, together with their respective dependent claims, clearly define over the cited prior art, and reconsideration and allowance of this application is respectfully requested

In view of the foregoing, entry of the present amendments and examination of the above-identified application on the merits in due course, are respectfully requested.

Kindly charge any additional fees due, or credit overpayment of fees, to Deposit Account No. 01-2135 (501.39835CX1).

Respectfully submitted,

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